ABSTRACT

A process for forming a conductive via in an integrated circuit structure that includes a first dielectric layer overlying a first conductive layer. A via cavity is formed in the first dielectric layer, which exposes the first conductive layer. A titanium nitride liner layer is formed in the via cavity, and the titanium nitride liner layer is exposed to an isotropic plasma containing hydrogen ions, thereby densifying the liner layer. A second conductive layer is formed adjacent the titanium nitride liner layer in the via cavity, which second conductive layer substantially fills the via cavity to form the conductive via. The via cavity is selectively etched with a hydrogen containing plasma prior to forming the titanium nitride liner layer. The plasma etch at least partially removes residue in the bottom of the via cavity, including carbon and oxygen.

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